(12) UK Patent Application (19) GB (11) 2 362 037 (13) A

(43) Date of A Publication 07.11.2001

(21) Application No 0010730.0

(22) Date of Filing 03.05.2000

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(51) INT CL^7
H05K 3/46 3/02 3/40

(52) UK CL (Edition S)
H1R RAD RAL R10 R22
B5N N0712 N175 N176 N178 N18X N181 N199 N20Y N206 N207 N211 N224 N3120 N384 N518 N613 N615 N618 N622 N648 N649 N658 N66Y N661 N671 N673 N68Y N776
U1S S2087

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JP 100027966 A **US 5837355 A** **US 4180608 A**

(58) Field of Search
UK CL (Edition S) **H1R RAD**
INT CL^7 **H05K 3/46**
Online: WPI, JAPIO, EPODOC

(54) Abstract Title
Printed circuit board manufacture

(57) A multi-layer printed circuit board is manufactured by applying a thermosetting resin in liquid form to a circuit board core, the resin is then partially cured to the "B" stage. A prepreg or resin coated conductor is then applied to partially cured resin layer. Using a partially cured resin in the lamination process reduces the occurrence of voids and improves adhesion between the layers. Methods of using stencil masks and conductive inks for interconnecting circuitry of a multilayered circuit board using via connections are also claimed.

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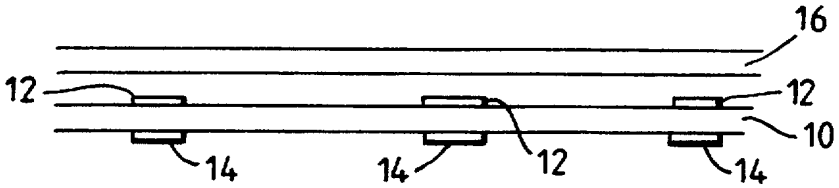

Fig. 1(A)

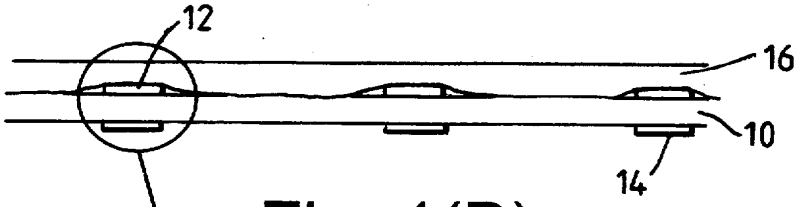

Fig. 1(B)

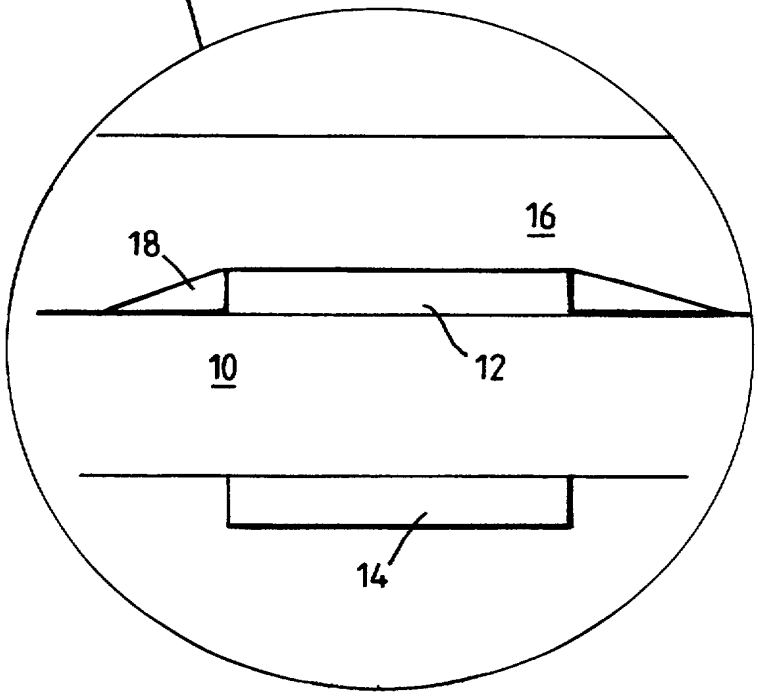

Fig. 1(C)

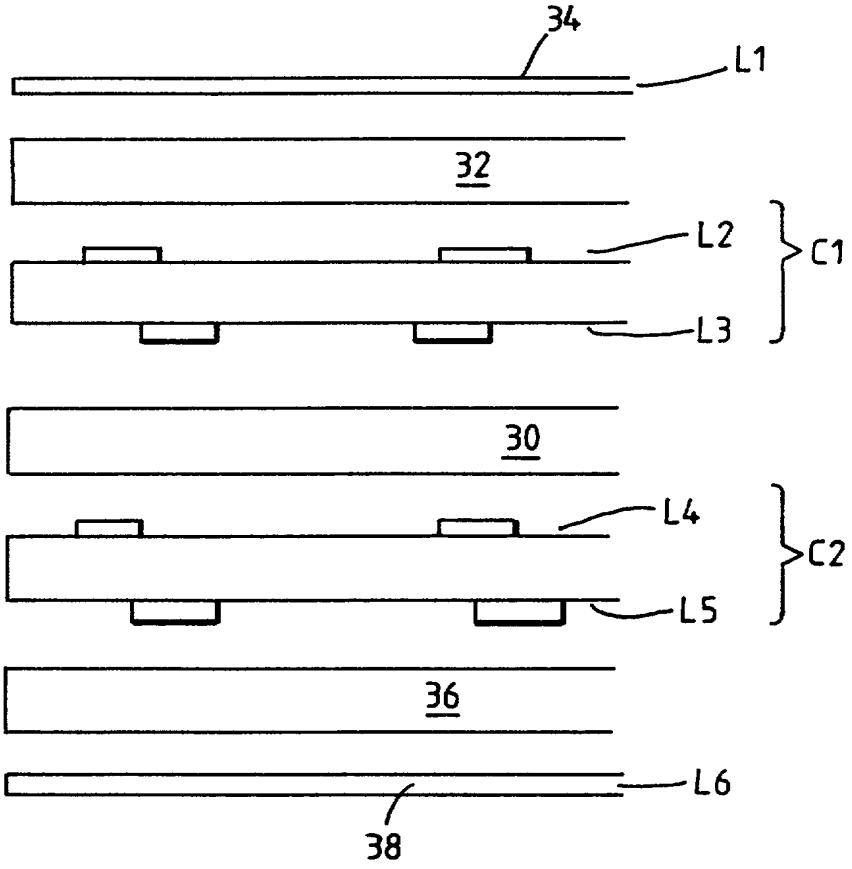

Fig. 2(A)

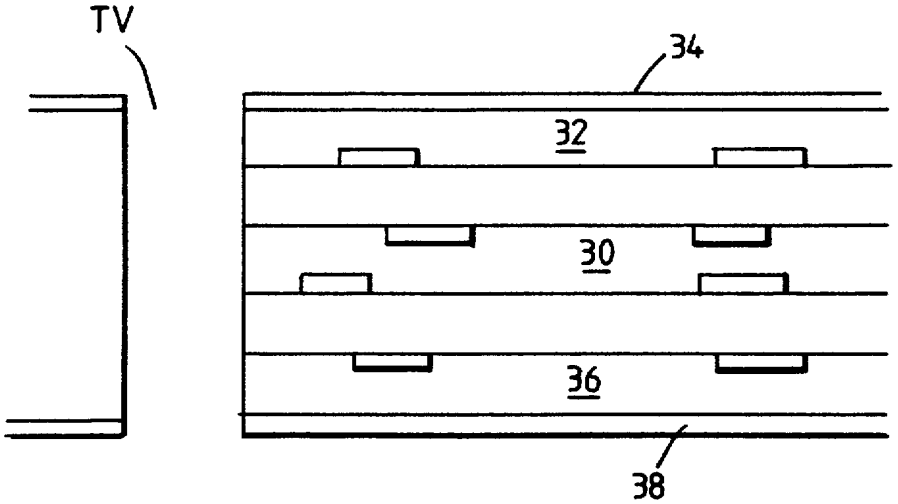

Fig. 2(B)

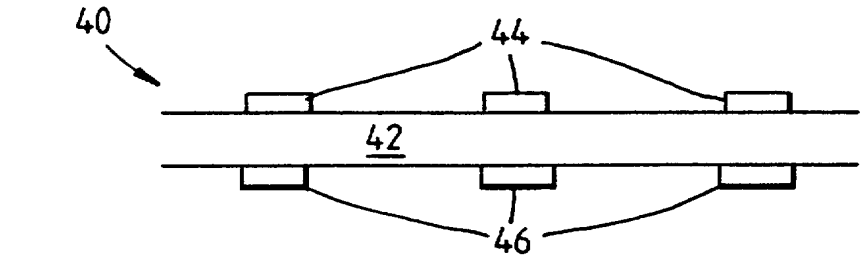

Fig. 3(A)

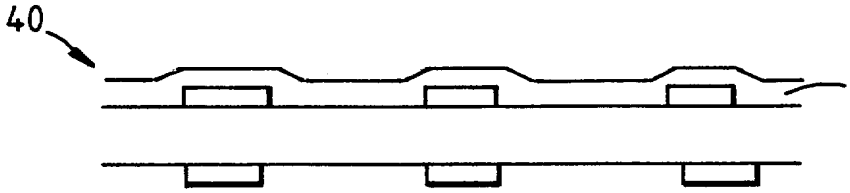

Fig. 3(B)

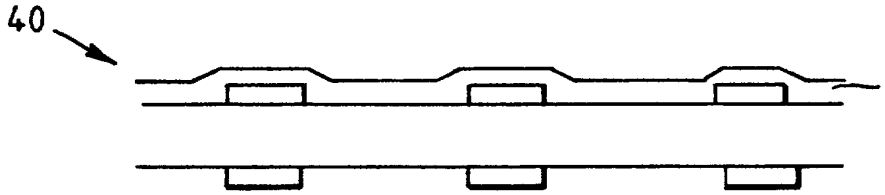

Fig. 3(C)

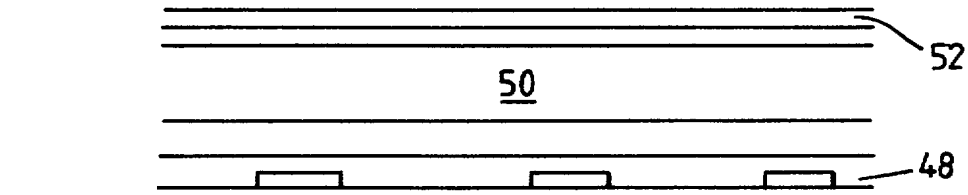

Fig. 3(D)

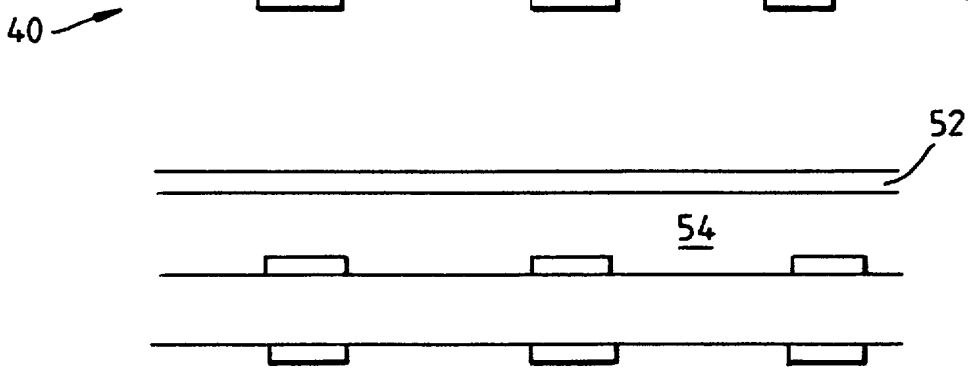

Fig. 3

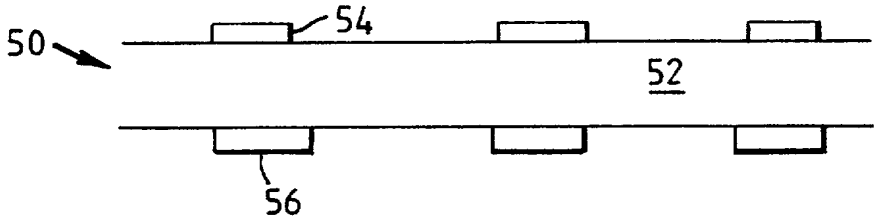

Fig. 4(A)

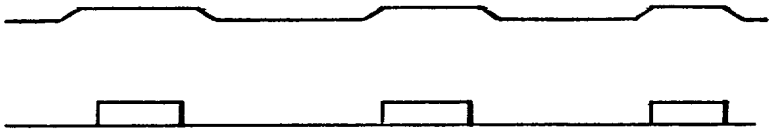

Fig. 4(B)

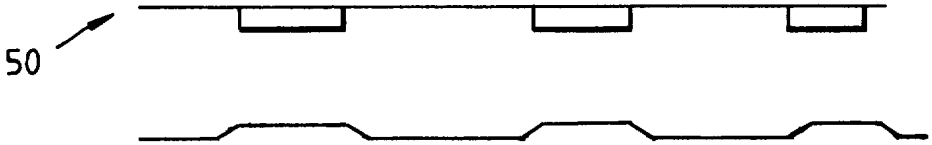

Fig. 4(C)

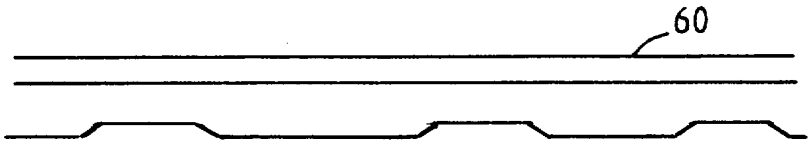

Fig. 4(D)

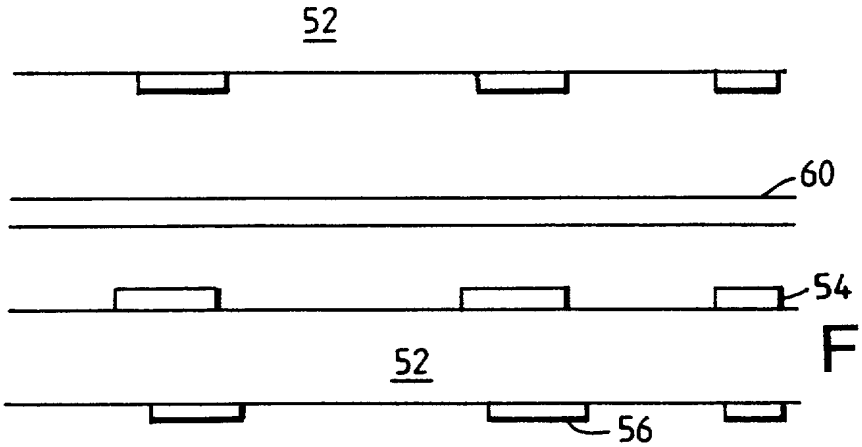

Fig. 4(E)

Fig. 4

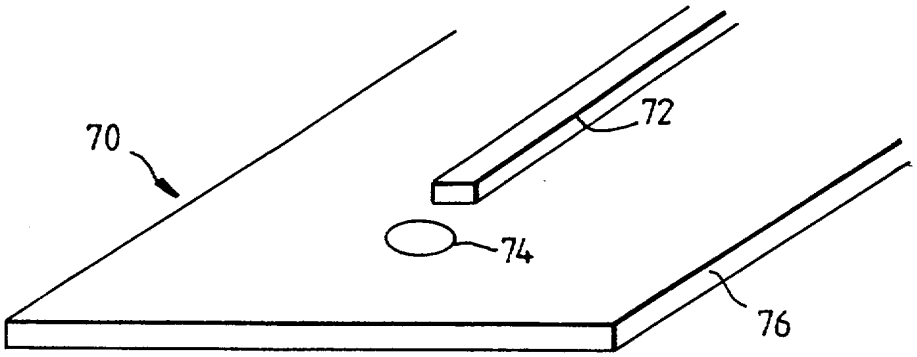

Fig. 5(A)

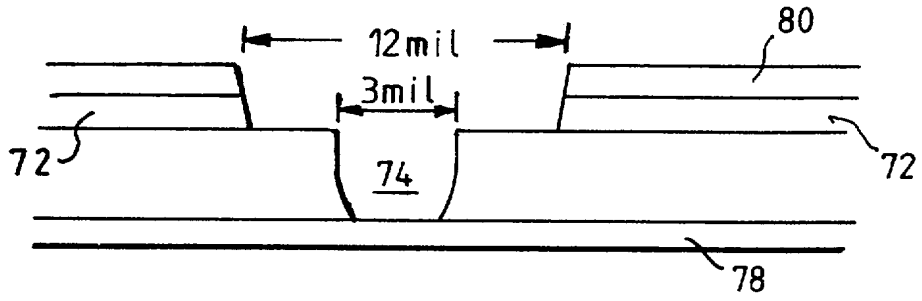

Fig. 5(B)

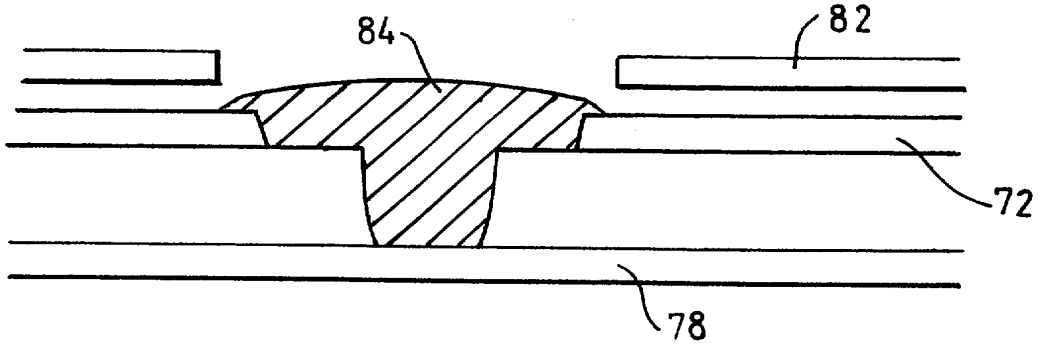

Fig. 5(C)

PRINTED CIRCUIT BOARDS

The present invention relates, in particular, to the making of high density printed circuit boards with, inter alia, microvias.

Printed circuit boards (PCBs), comprising of an insulating board carrying conductor traces of conductive material, have been used for many years to carry electronic circuitry. As the input and output densities of electrical components has increased, the number of interconnections in a given area of printed circuit board has also increased. One method of addressing this problem is for a conductive pattern to be provided on both sides of the board. The conductors extending from components are either soldered to both top and bottom of the board or connected by means of plated through holes. A printed circuit board with plated through holes requires mechanical drilling and the conductors on the top and bottom surfaces of the board are connected by a plated conductor layer provided on the hole sidewalls.

However, with the recent advances in digital circuitry , the increase in electrical component device speeds, the need for increased interconnection density and the consequent increase in the area density of electrical components, double sided printed circuit boards have become technologically inadequate.

In order to address these requirements, multilayer printed circuit boards were developed. This is similar to a "sandwich" of patterned conductors and insulating layers. Multilayer boards, commonly provide 4, 6 or 8 layers of conductors. However, notwithstanding this, the increased "clock speed" requirements of today's electronic devices require smaller area boards with even more layers. Furthermore, due to the lower power requirements of electronic products, the conductive line widths and the line spacing between conductive tracks has reduced drastically. There is also a need to reduce the inner layer line widths and via hole diameters that join different conductive layers on the boards. Mechanical drilling of via holes has been replaced by other techniques such as laser drilling which is capable of producing via hole diameters smaller than 10 mils

(1 mil = $^{1}/_{1000}$ inch). As multilayer circuit boards are made even more compact, difficulties arise during manufacture. Board warpage can occur during processing which may lead to assembly problems when automated component placing and soldering techniques are used. Another major problem is delamination where there is a bonding failure between the layers of the board, particularly during multiple heat exposures, for example , during hot air leveling and automated assembly soldering processes. Further problems are the high costs and long process cycle times associated with traditional methods of manufacturing multilayer boards.

It is an object of the first aspect of the present invention to provide a method of making a multilayer printed circuit board that can solve at least the first and second of the above disadvantages (board warpage and delamination).

According to the first aspect of the present invention, there is provided A method of manufacturing a multilayer printed circuit board, comprising the following steps: forming an inner core having circuit patterns on at least one side thereof, applying resin in liquid form to at least one side of the core, and pressing a prepreg or resin coated conductor to the core.

This new method can reduce or eliminate the problems of board warpage and delamination associated with the prior art technique that is now described with reference to Figure 1 of the accompanying drawings.

In Figure 1(A) an insulating board 10 is provided with circuit patterns 12 on the top side and circuit patterns 14 on the bottom side. These are produced using conventional techniques, which will not be described in further detail here. The patterns are given an oxidation treatment as is normally done before pressing the various layers together. Insulating layer 16 as shown in Figure 1(A) is a layer of prepreg. Prepreg is an abbreviation for preimpregnated material which consists of glass fiber which is impregnated with liquid resin and then dried but not fully cured. Above prepreg layer 16 is a copper layer 17.

The physical states of the resins used in printed circuit board construction will now be described. In stage "A" the resin is in liquid form and carried by a solvent. It usually has a shelf life of between 6 to 12 months. In stage "B", the resin has been typically heated to a temperature of approximately 180^0 C (+/-10^0 C) for a period of between one and three minutes ,enough to evaporate the solvent. This is called the "drying" or "baking" solvent removal process. In stage "B" the resin is not fully cured but is solid and "tacky". The molecular crosslinking of the resin has not started at this stage. Resin in stage "B" is prone to moisture absorption from the environment and must be kept in temperature and humidity controlled conditions. The shelf life of "B" stage resins typically does not exceed three months. In stage "C" the resin is typically heated to a temperature of approximately 180^0 C (+/-10^0 C) for a period of 45 to 55 minutes , resulting in the resin being fully cured, having reached the glass transition temperature. The process necessary to convert the resin from stage"B" to stage"C" is dependent upon the type of resin. Most commonly utilised is thermally cured resin, which is the type assumed in the following examples. However, there are also chemically-cured and photoimageable types of resins which may equally be appropriate.

No particular types or brands of resins are disclosed as relied upon in the following paragraphs since the various aspects of the present invention are not concerned with, or limited to, particular types of resin. A suitable resin would be Dow Chemical P/No. DER530A80, SHELL Part no. 1124A80, however, the fabricator can readily select the appropriate type of resin for each of the described processing stages, be it heat-cured, chemically-cured, photo-cured or whatever. The inventor has used the following resin composition in these inventions. For 100Kg of working resin, the composition consisted of; 80Kg DER530A80; 13.6Kg Ph powder; 3.2Kg Borden UV Block; and 3.2Kg of Dow Chemical XUS92505. The curing agent utililised could also be Dicy or 2e4mz (4- Imidazole) or similar type curing agents.

The insulating board, prepreg and copper layers shown in Figure 1 (A) are pressed together in a heated vacuum assisted hydraulic press which results in the buildup arrangement shown in Figure 1(B). Typically both sides of the core will be pressed together with prepreg

simultaneously but only one side is shown for clarity. The application of heat and pressure has caused the resin in the prepreg to flow and fill in the gaps and spaces between the circuit patterns on the surface of the insulating board and make the resin set to stage "C". However, this current state of the art process has drawbacks and, the present inventor believes, these are the major contributory factors that causes board warpage and de-lamination.

Figure 1(C) shows an enlarged view of part of Figure 1(B) showing resin layer 16 after pressing, the insulating board and the conductive pattern 12. The height of the conductive pattern is typically 1.4 mil high or 2.8 mil high (corresponding to 1 oz/per square foot and 2oz/per square foot copper foil respectively). The pressure applied is typically between 15 to 20 kg/cm^2 depending on the weight of the copper. ½ oz copper per square foot will require a pressure of about 15kg/cm whereas 2oz per square foot copper will require a pressure of about 20kg/cm for a similar type of prepreg. It is believed that the resin may not completely fill in the gaps between conductor patterns which can lead to voids as shown at 18. The trapped air and moisture can expand later, when the board is heated during processing, and cause delamination. Even the utilization of high vacuum during the pressing stage cannot completely eliminate trapping of air and moisture. The flow of resin under extremely high pressures may induce stress on the fiber glass which may cause board warpage and severe dimensional changes especially when there is a assymetrical and unbalanced circuitry design on the board.

Under extremely high pressure, excessive resin flow will cause possible resin starvation. This occurs when there is too much resin flow out of the board surface into the conductor patterns which leaves the fiberglass exposed with little resin content; a condition known as "dry ply". This condition can also cause delamination. Also, resin starvation can result in there being insufficient resin to ensure a smooth surface. This will pose some difficulties in forming the fine line conductive traces precisely.

To remedy those problems, in accordance with the first aspect of the present invention an additional step is provided of coating the circuitized insulating board with a liquid resin layer before the board

is laid up with prepreg and pressed. The liquid resin layer is dried to stage "B" to facilitate subsequent processing. This step gives an even layer on the outer surfaces of the insulating board before the placement of prepreg. Lower pressures may be used in the pressing step which reduces the stress induced in the fiberglass . Because the additional layer is applied in liquid form (stage "A") it can readily flow into all of the gaps in the circuitized board so that little or no air or moisture is trapped and voids are minimized or eliminated. Other problems such as resin starvation are also eliminated.

Glass Fiber type materials , suitable for laser drilling are also now available so the microvias discussed below can still be used with boards produced by this technique.

The steps of applying the resin in liquid form and drying the resin to Stage "B" may be done prior to the pressing of additional layers thereto. The reason being that once the copper is oxide treated , the circuitized patterns are extremely prone to damage. The protection afforded by the application of a resin layer dried to Stage "B" can reduce the likelihood of damage to the circuitized patterns and result in better production yields .

In a preferred embodiment of the first aspect of the present invention , the solid resin layer consists of prepreg. While it is possible to use other types of resin material, it is preferred to use prepreg because fiberglass improves the structural stability of the board, particularly in the manufacture of PCMCIA type printed circuit boards.

In a further preferred embodiment the inner core has a circuit pattern on both sides and the application of resin is done on both sides of the core. The resin is dried to "B" stage so that the board can be turned over and the liquid resin is then applied to the other side of the board. The drying time for the resin that is coated on the first side may be shortened because it will be further dried when the resin on the other side is dried.

While the first aspect of the present invention addresses the problems of board warpage and ,air and moisture entrapment that may result in delamination and resin starvation, it still requires the

use of resin layers dried to stage "B", the addition of a layer of prepreg (or RCC) followed by the lamination of a final layer of copper foil. Storage of prepreg causes significant production difficulties because it is prone to moisture absorption and therefore its shelf life is limited to approximately six months from the date of manufacture. Consequently, special storage and handling procedures must be followed. The use of prepreg increases the number of and complexity of the process steps in the manufacture of the board, particularly in situations where in mass production, the manufacturer is required to produce batches of boards with specifications requiring different thicknesses of prepreg.This can cause substantial disruption to an automated production line and this leads to increased production costs .

It is an object of the second aspect of the present invention to further address this problem.

According to a second aspect of the present invention there is provided a method of making a multilayer printed circuit board, with the following steps involved:

-Forming a circuit board core having a patterned surface on at least one side,

-Coating the patterned surface with a thermosetting resin in liquid form,

-Drying the resin to stage "B",

- Forming a conductive layer on the resin, and

-Curing the resin to stage "C".

The application of liquid resin in this aspect of the invention will typically require application of a thicker layer of resin than that of the first aspect (Usually, the thicknesses can range between 1mil to 5mil). The reason for this is that the next conductive layer is applied directly on top of the resin (without any intervening layer such as prepreg) and so it must provide adequate spacing between the conductive layers on its own to prevent short circuits.

US Patent 5 948 280 describes a two step process in which a first layer of resin is applied in liquid form. This layer is cured (to stage "C") and a second layer of liquid resin is applied to the first layer of

resin and dried (to stage "B"). A conductive layer is then hot pressed onto this second layer. Whilst this would appear to address the problem of storage and material handling of stage "B" material by eliminating the use of prepreg at this stage in the manufacturing process, it is not appropriate in mass production. For example, a double sided board will require more than four separate resin coating and curing steps (although, the last two curing steps can occur simultaneously) to apply two further layers to the board. Not only are these steps time consuming but they also give problems in that the molecular structure of the outer resin layer will not have complete crosslinking with the inner resin layer because the first layers of resin have already been fully cured to Stage "C". Besides, additional processes like heating are commercially non-viable. They cause disruption to automated line processing in mass production mode. Excessive heating and reheating and too many curing steps are also undesirable as it makes the resin extremely brittle and susceptible to cracking and delamination. Another problem is that when the board is drilled, the holes are not clean. Experiments have shown that the knee of a laser-drilled hole is often chipped because of inadequate crosslinking of the lower resin layer. This prior art patent also discloses the use of ½ oz/square foot copper , having a thickness of 0.7 mil. However, 1oz. Copper is used more often which has a thickness of 1.4 mil. The process described in US patent 5 948 280 requires the application of resin by silk screening . Experiments have shown that this method of application of resin is limited to achieving a coating of resin of 0.7mil (after curing).Two coats would therefore produce a resin layer thickness of 1.4mil. This method when applied to a 0.7 mil conductive track may not have sufficient insulation between the conductive layers. If 1.4mil track is utilized, then two coats as described in the patent would be insufficient. A minimum of 3 coats would be required. This would exacerbate the problems associated with multiple heating of the board that is required to cure the subsequent layers of resin and would increase production costs.

By contrast, the process according to the second aspect of the present invention requires only a single application of liquid resin and consequently, the problems associated with poor crosslinking and brittleness caused by repetitive thermal processing steps are virtually eliminated.

In preferred embodiments of the second aspect of the present invention the resin is applied to both sides of the core simultaneously.

The desire for increased device speeds and interconnection density, has, as mentioned above, resulted in the need for smaller via holes , typically measuring only 3 mil in diameter. A mechanical drill is unsuitable in this case because the precision of controlled depth drilling is inadequate. These holes are typically made by laser drilling, plasma drilling , photoetching and other high precision techniques. However, these techniques suffer from the disadvantage that they cannot effectively drill through copper or other conductive layer material. Consequently, there is a need for the copper to be removed by etching prior to the forming of the via holes. This requires additional photoprinting and etching steps for the formation holes in the copper which results in long processing time and high costs.

It is an object of the third aspect of the present invention to solve this problem.

According to a third aspect of the present invention there is provided a method of making interconnections in the inner layer of a multilayer circuit board, the method comprising etching circuit patterns on a conductive layer, wherein the conductive layer has at least one further conductive layer beneath it, forming via holes as far as the next conductive layer, and filling the via holes with conductive material using a stencil mask to create the interconnection between the conductive layers.

According to a fourth aspect of the present invention there is provided a printed circuit board comprising a plurality of layers of conductive patterns, at least two layers of the board being electrically connected by interconnections composed of cured conductive ink.

The background to the third and fourth aspects of the present invention will now be discussed with reference to Figure 2 of the accompanying drawings.

Figure 2(A) shows a conventional technique for preparing a six-layer board. Two double-sided board cores C1, C2 are first prepared using any suitable technique and these are used to provide conductive layers L2, L3 and L4, L5 respectively. These inner cores are then laid up with a layer of prepreg 30 between them (which usually will comprise between 2 and 8 plies of prepreg depending on the required finished thickness), a ply of prepreg 32, a layer of copper foil 34 (which will become layer L1), another ply of prepreg 36 and another layer of copper foil 38 (which will become layer L6). The whole assembly is then hot pressed together to cure the various prepreg layers to Stage "C". Figure 2(B) shows the six layer board after pressing.

However, this current art technique has significant drawbacks for the manufacture of circuit boards intended for high component density circuitry. Perhaps the most significant is that it is impossible to accurately create buried vias (electrical interconnections between conductive layers) between the layers L3 and L4 . A buried via is an inter-layer connection that does not extend to the outer layer of the board. A related interconnection is the blind via which is drilled without extending beyond the outer layer of the board. A blind via is equally impossible to apply between layers L3 and L4. The only type of interconnection which can join layers L3 and L4 is a through-hole which, as its name implies, extends all the way through the board. There must generally be drilled using a mechanical drill which has a minimum diameter of approximately 12 mils. In addition to having a large diameter, such a hole must extend through all of the layers of the board, which seriously reduces the space available for circuit connections.

An alternative technique is the so-called "sequential build" which starts with a single core and adds one or two conductive layers to the external faces of the inner core at each processing step. This gives access to all of the layers during build-up and allows blind vias to be generated between any adjacent layers of the board. These vias will typically be laser drilled and will occupy only 3 mil diameter areas on each layer. However, since laser drilling cannot effectively cut through copper, a drilling window or copper opening with diameters usually greater than the required diameter of the hole, must first be created in the copper surface by etching to expose the resin layer

beneath. Once the laser via has been drilled, the via hole and the adjacent resin areas are electroplated with copper. A second etching step is then required to create the conductive tracks. The sequential processing technique is currently unpopular, owing to its high manufacturing cost.

The technique in accordance with the third aspect of the present invention, however, removes the need for the second etching step, since the artwork registration, imaging and etching process of each conductive surface needs to be performed only once. This is a complex precision process which requires extremely accurate tooling holes to ensure precise registration of artwork particularly when the process has to be repeated twice . In contrast, the technique in accordance with the third aspect of the present invention, replaces the second etching step with the formation of a conductive interconnection by a printing method. The cumulative processing time for the inner layers of the printed circuit board is reduced by as much as 50% when compared with the well known sequential build technique using blind vias.

In a preferred embodiment of the third aspect of the invention the conductive material is printed and in a still further preferred embodiment the printing method is by silk screen printing. The conductive material is preferably a conductive ink and, still further preferably, a carbon ink such as Electra low resistance carbon ink ED 5601.

The fourth aspect of the invention comprises a printed circuit board having vias formed in accordance with the third aspect using a conductive ink.

The present invention will now be described by way of non-limiting examples, with reference to the accompanying drawings, in which:

Figure 1 shows a the prior art technique for pressing a layer of prepreg onto an inner core,

Figure 2 shows a prior the prior art technique for laying up a six-layer circuit board,

Figure 3 shows a series of steps illustrating an embodiment of the first aspect of the invention,

Figure 4 shows a series of steps illustrating an embodiment of the second aspect of the invention, and

Figure 5 shows a series of steps illustrating an embodiment of the third aspect of the invention.

Figure 3(A) shows circuit inner core 40 comprising an insulating board 42 with a circuit pattern 44 on an upper surface thereof and a circuit pattern 46 on a lower surface thereof. This circuit inner core can be prepared using any suitable techniques and these will not be discussed further here. The height of the circuit pattern above the board 42 will typically be 1.4 mil (1 oz. copper) or 0.7 mil (1/2 oz. copper).

The upper surface of the core 40 is then treated with a setting resin in stage "A", in other words in liquid form. The object is to smooth out the bumps on the surface of the inner core caused by the circuit pattern. The thickness of the layer of resin applied will depend on the thickness of the circuit pattern. This will differ according to the copper weight utilized. For example, 1oz copper will require a thinner coating ,typically 2 mils whereas 2oz copper may require an even thicker coating, typically 3 mils. To achieve this, the apparatus used in this embodiment of the invention allows the application of a variable thickness of resin from 1 mil to 5 mil. Various techniques are suitable for the application of this layer such as curtain coating, roller coating, spray coating and bar coating. Of these, curtain coating is preferred because it provides an accurate , uniform layer with thickness of between 1 to 5 mils in a single application.

In addition to the techniques listed above, screen printing may be used to apply the resin layer in this case but only for layer thicknesses towards the lower end of the range.

Figure 3(B) shows the core 40 after application of the resin layer 48.

Figure 3(C) shows the drying step in which the resin applied in Figure 3(B) is dried to stage "B". This step is performed if two sided operation is required. By drying a resin layer applied to a first side, this layer becomes sufficiently stable to allow the board to be turned over and the process to be repeated on the other side.

Figure 3(D) shows the inner core laid up with a layer of prepreg 50 (which may either contain glass fiber or glass fiber suitable for laser drilling) and a layer of copper foil 52. Only one side of the board core is built up as shown for clarity. In practice both sides would be laid up before pressing. The board is then pressed together with the application of heat to cure the prepreg layer 50 and the resin layer 48. Since a lesser amount of resin is required to fill gaps and spaces to bond to the inner core, the pressure applied can be significantly reduced – typically to a value of 5 to 15 kg/cm^2.

Even resin coated copper (RCC), which typically requires lower pressures than a combination of prepreg and copper foil, can be more readily pressed using this technique. In this case RCC replaces the separate layers of prepreg and copper foil at the lay-up stage. This provides less distortion of the copper layer in the RCC with consequent advantages for the processing of the circuit pattern applied thereto.

One advantage of using RCC is that, because there is no glass fiber , the resulting board can be laser drilled. However, prepreg having glass fiber suitable for laser drilling is now available and so this advantage is no longer so important for some applications.

An embodiment according to the second aspect of the invention will now be described with reference to Figure 4.

Figure 4(A) shows an inner core 50 comprising an insulating board 52, top circuit pattern 54 and bottom circuit pattern 56 similar to the arrangement shown in Figure 3(A). Again a layer of resin in liquid form (stage "A") is applied to the upper surface of the board inner similarly to the embodiment of the first aspect of the invention. Usually, however, the thickness of the layer will be greater than in that embodiment, typically from 1 to 5 mils and preferably 3 mils.

Figure 4(B) shows the board core and resin layer on the top side. The resin layer is then dried (to stage "B") as shown in Figure 4(C). While only one-sided processing is illustrated in Figure 4, two-sided processing can readily be provided by repeating the application of resin and the drying steps for the other side of the inner core (either simultaneously or after inverting the board). The lay up of a copper layer 60 illustrated in Figure 4(D) would then be repeated on the underside. The whole arrangement is then hot pressed to cure the resin layer to stage "C"and the result is shown in Figure 5(E). The pressure required will typically be 3 to 7kg/cm^2.

This low pressure and single curing stage virtually eliminates the risk of distortion of the board but there are significant other advantages as well. Firstly, by eliminating the use of prepreg (which necessitates cutting to size and labour intensive laying up) the invention allows lamination to be incorporated into a continuous automated inline production process which avoids the necessity and cost of retaining stocks of sheets of prepreg. Secondly, by eliminating the use of prepreg, the resin layer can readily be drilled by laser to form the micro vias (although glass fibers that can be laser-drilled are now available). Thirdly, the resin is considerably cheaper than prepreg so the cost of the overall process is reduced. Fourthly, the dielectric constant of a pure resin layer is lower than that for a layer of prepreg (prepreg has a high dielectric constant due to the mix with glass fiber which has a characteristic high dielectric constant) which leads to an increase in the signal propagation velocity.

An embodiment according to the third and fourth aspects of the invention will now be described. In order to place the benefits of this embodiment in context, the known technology will be discussed first.

The sequence of steps required in the known sequential build-up using laser-drilled buried vias will now be described. It is assumed that a core has been produced (whether this has two layers or comprises a previous stage in production) and that the surface copper pattern has been oxidized or otherwise prepared for etching; The process steps are as follows:

1. Dry film is applied to the copper layer
2. Artwork is registration is done .
3. The dry film is exposed.

4. The dry film is developed.
5. Copper is etched to create a drilling window that exposes the resin layer .
6. Dry film is stripped.
7. Laser drilling of the resin/prepreg follows but not through the inner layer copper.
8. Plating of the holes with electroless copper is done to create the via connections
9. Second dry film is applied to the copper layer
10. Second Artwork registration is done
11. The dry film is exposed
12. The dry film is developed.
13. Copper is plated
14. Tin plating is done
15. The dry film is stripped .
16. Copper is etched to create the circuitry

The present inventor has realized that the processing time can be virtually cut in half by using a different technique to generate the vias. In addition, the dry film used twice in the above process as an etch resist layer is expensive and so there are significant cost savings also from using this new technique.

Figure 5(A) illustrates the procedure in general terms. Only one resin layer is shown for clarity. A mask (not shown) is first used to etch a copper layer in one step. This removes both the unwanted copper (to generate the circuit tracks) and the copper that lies above the locations of the desired via holes. Track 72 that is to be connected to a via is interrupted by this process and a hole 74 is laser drilled in the resin layer 76. Because the laser beam will not penetrate copper (or can be arranged not to do so by controlling the depth the laser drills to by careful selection of parameters such as the pulse widths and frequency), the hole ends accurately at the next layer of copper.

This is illustrated in the sectional view of Figure 5(B) where the hole 74 terminates at the copper layer 78. Also shown in this view is a mask 80 that has been used to define the extent of the etching of the copper. The diameter of the hole in the mask (and hence the diameter of the hole in the copper layer) may be as much as 3 to 4

times the diameter of the laser drilled hole. The reason is as follows. During processing, printed circuit boards are subjected to great thermal stresses and they expand and contract as a result. If a board of length 24 inches expands by only 0.001% this results in parts of the board being 2.4 mil from where they should be. By providing a larger hole in the copper (and additionally a large "target area" in the copper layer below) mis-registration of the laser drill with respect to the board can be accommodated. The mask 80 is removed between the etching step and the following step described with reference to Figure 5(C) .

The conductive material is applied by means of screen printing on the surface of the board 82. The screen printing is done using a mesh of of 80T / inch monofilament polyester. The stencil material may be red T1 or indirect film or direct photostencil system with a thickness of 120-125 u. For automated printing, the screen tension may be about 22-28 Nt/cm with a squeegee hardness of about 65 durometer . Offcontact may be about 3/16" and the pressure may be 45-60 psi for both front and back.

The stencil is provided with openings only above the via holes 74 . The remainder of the circuit pattern is protected from contamination by the conductive material which is then printed onto the board using Mask 82 . Suitable conductive material is a thermally cured carbon ink available from Electra under Part # ED 5601.

This results in a conductive formation 84 connecting the copper layer 78 and the copper layer 72 and which becomes permanent when the ink is baked in an oven .

The present inventor has successfully filled holes of approximately 3 mils in diameter and 3 mils in depth. Holes with a higher aspect ratio than this may not necessarily be filled correctly and so the resulting via hole may fail. The key to this aspect of the invention is the use of a screen printing stencil for applying the conductive material.

The series of steps carried out in accordance with an embodiment of the third aspect of the invention is as follows. By comparison with

that above, the benefits of this aspect of the invention can readily be appreciated.

1. Dry film is applied.
2. Artwork registration.
3. The dry film is exposed.
4. The dry film is developed .
5. The copper is etched to create the circuitry.
6. The via holes are laser drilled.
7. The via holes are given a desmear treatment.
8. Carbon ink is applied by screenprinting .
9. Carbon ink is cured by baking at 150 deg C for 50 minutes.

Because of the elimination of the second photoimaging and etching process steps , the production process for inner layers requiring laser drilled blind or through vias is simplified such that the number of production steps are substantially reduced. This process is both faster and cheaper (due to the savings made in chemicals, copper utilization and time) than the previous two stage artwork registration,imaging and etching.

Although carbon ink has been described as an example ,the conductive material can comprise a wide range of materials including, but not limited to, silver , copper , tin,and lead pastes,

CLAIMS:

1. A method of manufacturing a multilayer printed circuit board, comprising the following steps:
forming an inner core having a circuit pattern on at least one side thereof,
applying resin in liquid form to at least one side of the core, and
pressing a prepreg or resin coated conductor to the core.

2. A method as claimed in claim 1, further comprising a step of drying the resin in liquid form to stage "B" before applying the prepreg or resin coated conductor .

3. A method as claimed in claim 1 or claim 2, wherein the solid resin layer comprises prepreg.

4. A method as claimed in claim 1 or claim 2, wherein the solid resin layer comprises a resin coated conductive layer.

5. A method as claimed in any one of the claims 1 to 4, wherein the core has a circuit pattern on both sides thereof and wherein the step of applying a resin comprises a step of applying a resin in liquid form to both sides of the inner core.

6. A method as claimed in claim 5, wherein the step of applying a resin in liquid form to both sides of the core comprises applying a resin to a first side of the core followed by drying to stage "B" and applying a resin to a second side of the core followed by drying to stage "B"

7. A method as claimed in any one of claims 1 to 6, wherein the step of applying a resin in liquid form is carried out using screen printing, roller coating, curtain coating, spray coating or bar coating.

8. A method as claimed in claim 7, wherein the step of applying the resin comprises curtain coating the resin.

9. A method of making a multilayer printed circuit board, comprising the following steps:

-Forming a circuit board core having a patterned surface on at least one side,
-Coating the patterned surface with a thermosetting resin in liquid form,
-Drying the resin to stage "B",
- Forming a conductive layer on the resin, and
-Curing the resin to stage "C".

10. A method as claimed in claim 9, wherein the conductive layer is a layer of conductive foil and the method further comprises a step of etching the conductive layer after curing the resin.

11. A method as claimed in claim 9 or claim 10, the circuit board core having a circuit pattern on both sides thereof, wherein
the step of coating the circuitized surface with a setting resin in liquid form comprises coating both sides of the circuit board core.

12. A method as claimed in claim 11, wherein the step of applying a resin in liquid form to both sides of the inner core comprises applying a resin in liquid form to both sides of the inner core sequentially.

13. A method as claimed in claim 11, wherein the step of coating both sides of the inner core comprises applying a resin to both sides of the inner core simultaneously.

14. A method as claimed in any one of claims 9 to 13, wherein the step of coating is carried out using screen printing, roller coating, curtain coating, spray coating or bar coating.

15. A method as claimed in claim 14, wherein the step of coating comprises curtain coating.

16. A method of making interconnections in the inner layer of a multilayer circuit board, the method comprising:
etching circuit patterns on a conductive layer, wherein the conductive layer has at least one further conductive layer beneath it,
forming via holes as far as the next conductive layer, and
filling the via holes with conductive material using a stencil mask to create the interconnection between the conductive layers.

17. A method as claimed in claim 16, wherein the step of filling the via holes with conductive material comprises printing the conductive material.

18. A method as claimed in claim 17, wherein the step of printing the conductive material comprises screen printing.

19. A method as claimed in any one of claims 16 to 18, wherein the step of forming via holes comprises a step of laser drilling, plasma etching, alkali etching or photoimaging

20. A method as claimed in any one of claims 16 to 19, wherein the conductive material comprises a conductive ink or paste.

21. A method as claimed in claim 20 wherein the conductive ink comprises carbon ink.

22. A method of manufacturing a multilayer printed circuit board comprising a method of making vias as claimed in any one of claims 16 to 21.

23. A printed circuit board comprising a plurality of layers of conductive patterns, at least two layers of the board being electrically connected by interconnections composed of cured conductive ink.

24. A printed circuit board as claimed in claim 28 wherein the conductive ink comprises carbon ink.

25. A method of manufacturing a printed circuit board substantially as herein described with reference to Figures 3, 4 or 5 of the accompanying drawings.

26. A printed circuit board substantially as hereinbefore described with reference to Figure 5 of the accompanying drawings.

Application No: GB 0010730.0
Claims searched: 1-8

Examiner: SJ Morgan
Date of search: 15 May 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H1R(RAD)

Int Cl (Ed.7): H05K 3/46

Other: Online: WPI, JAPIO, EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	US 5 837 355	(SUMTOMO) See whole document.	1-8
X	US 4 180 608	(DEL) See lines 13-35, column 2.	1, at least
X	JP 10 027 966 A	(TOSHIBA) See abstract.	1, at least

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Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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